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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/065,212	09/26/2002	Raj Kumar Jain	2000P19188US	8176

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EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 06/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/065,212	JAIN, RAJ KUMAR	
	Examiner	Art Unit	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13-16* is/are allowed.

6)☒ Claim(s) *1,17,20 and 23* is/are rejected.

7)☒ Claim(s) *2-12,18,19,21,22,24 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/05/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 07/05/2005 has been entered.

2. Claims 1-25 are presented for examination.

Information Disclosure Statement

3. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on 07/05/2005.

4. Information disclosed and list on PTO 1449 was considered.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1,20,23 are rejected under 35 U.S.C. 102(b) as being anticipated by Sartore et al. (U.S. Patent No. 5,887,272).

Regarding claim 1, Sartore et al. disclose an IC (Figure 3) comprising:

a memory cell array having a plurality of memory cells (Figure 3, 40), wherein the memory cells (Figure 3, DRAM) includes at least first and second ports forming a memory cell array with at least first and second access ports for accessing the memory cells (Column 5, lines 64-67).

a cache memory (Figure 1, 14) coupled to the first and second access ports, wherein during a read operation to the memory cell array to obtain read data through one of the first and second ports, the cache memory provides the read data if the read data is contained therein or the memory cell array provides the read data if the read data is not contained in the cache memory (Column 8, lines 48-55, in read cycle, if data stored in cache memory, loading data in main memory, if data is not in the cache memory, writing to cache memory, Column 16, lines 40-63, column 17, lines 15-33); and

a refresh control circuit (Figure 3, 68, REFRESH CONTROL) for performing refresh operations.

Regarding claim 20, Sartore et al. disclose an IC comprising a memory cell array (Figure 3) having a plurality of memory cells (Figure 3, 40) , wherein the memory cells includes at least first and second ports forming a memory cell array with at least first and second access ports (Column 5, lines 64-67, read port, write port), wherein at least one of the first and second ports are used for memory accesses (Column 8, lines 45-55); and a cache memory coupled to at least the access ports used for memory, the cache memory provides the read data if the data is contained therein or the memory cell

array provides the read data if the data is not contained in the cache memory (Column 8, lines 48-55, in read cycle, if data stored in cache memory, loading data in main memory, if data is not in the cache memory, writing to cache memory, Column 16, lines 40-63, column 17, lines 15-33).

Regarding claim 23, Sartore et al. disclose wherein the at least first and second access ports are used for memory access (Column 8, lines 49-55).

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

7. Claim 17 is rejected under 35 U.S.C. 102(e) as being anticipated by Rao (U.S. Patent No. 6,256,256).

Regarding claim 17, Tao discloses a IC (Figure 9) comprising a memory array having a plurality of memory cells (Figure 9, 401a) with at least first and second ports forming a memory cells array with at least first and second access ports (ABSTRACT, Figure 6), a cache memory (Figure 2A, 202) coupled to the first and second ports (Figures 2), the first and second access ports comprising address terminal and data

terminals, and the second access port being controlled by refresh control circuit to perform a refresh of the memory cells (Column 2, lines 15-42, Column 4, lines 60-65)

Allowable Subject Matter

8. Claims 2-12, 18-19, 21-22,24-25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 2-12, 18-19, 21-22,24-25 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Sartore et al. (U.S. Patent No. 5,887,272), and Rao (U.S. Patent No. 6,256,256), and others, does not teach the claimed invention having a tag portion, an address portion, and a data portion corresponding to each other, wherein the tag portion indicates if the corresponding address and a data portion contain valid address and data value as claims 2-12 disclosed, and wherein a refresh operation is performed for a row of memory cells through the second access port, and a read command received through the second access port is performed through the cache memory in parallel to the refresh operation as claim 18 disclosed, and a first and second selection transistors as claim 19 disclosed, and an arrangement of first and second ports as claims 21-22,24-25 disclosed.

9. Claims 13-16 are allowed.

Claims 13-16 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the

claimed limitations. Sartore et al. (U.S. Patent No. 5,887,272), and Rao (U.S. Patent No. 6,256,256), and others, does not teach the claimed invention having a switching device being operated to connected either one of the memory cell array and the cache memory to the at least of the access ports in response to a read operation as claims 13-16 disclosed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Thong Q. Le
Primary Examiner
Art Unit 2827